WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a first device formed on the insulating layer, including:

a first fin formed on the insulating layer, and

a first silicided gate formed over a portion of the first fin and including a first thickness of silicide material; and

a second device formed on the insulating layer, including:

a second fin formed on the insulating layer, and

a second silicided gate formed over a portion of the second fin and including a second thickness of silicide material different from the first thickness.

2. The semiconductor device of claim 1, wherein the first device further includes:

a first dielectric layer formed between the first fin and the first silicided gate, and

wherein the second device further includes:

a second dielectric layer formed between the second fin and the second silicided gate.

3. The semiconductor device of claim 1, wherein the first silicided gate is partially silicided and the first thickness ranges from about 100 Å to about 500 Å.

4. The semiconductor device of claim 1, wherein the second silicided gate is fully silicided.

5. The semiconductor device of claim 4, wherein the second thickness ranges from about 400 Å to about 1000 Å.

6. The semiconductor device of claim 1, wherein the first device is an NMOS device and the second device is a PMOS device.

7. The semiconductor device of claim 1, wherein the first device and the second device are included in a single circuit element.

8. The semiconductor device of claim 1, wherein a first threshold voltage of the first device is lower than a second threshold voltage of the second device.

9. A method of manufacturing a semiconductor device, comprising:

forming first and second fin structures on an insulator;

forming first and second gates over respective channel portions of the first and second fin structures;

partially siliciding the first and second gates; and

fully siliciding one of the first and second gates.

10. The method of claim 9, further comprising:

forming first and second dielectric layers on the first and second fin structures, respectively.

11. The method of claim 9, wherein the forming first and second gates includes: depositing a gate material over the first and second fin structures, and

selectively etching the gate material to define the first and second gates.

12. The method of claim 9, wherein the partially siliciding the first and second gates includes:

depositing a metal on the first and second gates, and

annealing the metal to partially silicide the first and second gates.

13. The method of claim 9, further comprising:

masking the first gate and the first fin structure, wherein the fully siliciding includes:

fully siliciding the second gate.

14. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a first device formed on the insulating layer, including:

a first fin formed on the insulating layer,

a first dielectric layer formed on the first fin, and

a partially silicided gate formed over a portion of the first fin and the first dielectric layer; and

a second device formed on the insulating layer, including:

a second fin formed on the insulating layer,

a second dielectric layer formed on the second fin, and

a fully silicided gate formed over a portion of the second fin and the second dielectric layer.

15. The semiconductor device of claim 14, wherein a silicided portion of the partially silicided gate has a thickness ranging from about 100 Å to about 500 Å.

16. The semiconductor device of claim 14, wherein the fully silicided gate has a thickness ranging from about 400 Å to about 1000 Å.

17. The semiconductor device of claim 14, wherein one of the first device and the second device is an NMOS device and another one of the first device and the second device is a PMOS device.

18. The semiconductor device of claim 14, wherein the first fin and the second fin are electrically connected.

19. The semiconductor device of claim 14, further comprising:

a third device formed on the insulating layer, including:

a third fin formed on the insulating layer,

a third dielectric layer formed on the third fin, and

a partially silicided gate formed over a portion of the third fin and the third dielectric layer, wherein

a silicided portion of the partially silicided gate formed over the portion of the third fin and the third dielectric layer has a different thickness than a silicided portion of the partially silicided gate formed over the portion of the first fin and the first dielectric layer.

20. The semiconductor device of claim 14, wherein a first threshold voltage of the first device is lower than a second threshold voltage of the second device.